Design and Simulation of Small Scale RF MTF-MOSFET

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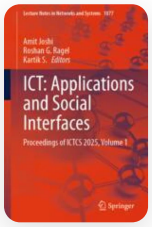

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Abstract

In this study, trenches inside the epitaxial layer are proposed as structural alterations to the traditional planar metal-oxide semiconductor field-effect transistor (MOSFET) on silicon-on-insulator (SOI) substrates. The innovative multi-trench-finger MOSFET (MTF-MOSFET) features multiple channels in its p-base, achieved by placing several vertical gates in distinct trenches. These additional channels enable parallel conduction of the drain current. TaN is used as the gate electrode and silicon dioxide (SiO2) as the gate dielectric in the suggested MTF-MOSFET architecture. The inclusion of multiple channels

significantly enhances the device's electrical characteristics. Specifically, the transconductance (gm) and the drain current (ID) are substantially increased due to the concurrent conduction of many channels. This concurrent conduction leads to a marked improvement in the cut-off frequency (fT). Two-dimensional simulations were used to assess and contrast the MTF-MOSFET's performance with that of a standard MOSFET. The results demonstrate that, with a gate length of 60 nm, the MTF-MOSFET exhibits: 6.5 times increase in ID, 3.7 times improvement in gm, 1.3 times enhancement in fT and superior control over short channel effects. These improvements underscore the significant advantages of the MTF-MOSFET design over the traditional planar MOSFET, particularly in terms of current handling, transconductance, frequency response, and mitigation of short channel effects. Proposed device is used for ICT Applications for Electrical and Intelligent Engineering.

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